AMENDMENTS TO THE TITLE:

Please amend the Title as follows:

SOLID STATE IMAGING APPARATUS INCLUDING MOS TRANSISTORS

AMENDMENTS TO THE SPECIFICATION:

Please amend paragraph [0021] as follows:

[0021] First, a transfer transistor **1102** (for example, in the upper pixel in FIG. **12**) in a row of a pixel array in which a signal accumulated in a photodiode **1101** is to be read out is turned on, and the read signal charges are accumulated in a floating diffusion. The accumulated signal charges are converted into a voltage using an amplifier transistor **1104**, and the converted signal charges are externally read out as a pixel signal by turning a select transistor **1105** on. Next, the signal accumulated in the floating diffusion is ejected by turning a reset transistor **1103** on and returned to an initial state. Subsequently, a transfer transistor **1102** (for example, in the lower pixel in FIG. **12**) in a column of the pixel array in which a signal is to be read out is turned on, and the read signal is transferred to the floating diffusion. Subsequent operations of the reset transistor **1103**, the amplifier transistor **1104** and the select transistor [[**1102**]] **1105** are the same as in the description of the upper pixel.

Please amend paragraph [0025] as follows:

[0025] Next, a signal accumulated in the floating diffusion is ejected by turning a reset transistor **1103** on and returned to an initial state. Subsequently, a transfer transistor **1102** (for example, in the lower pixel in FIG. **13**) in a column of the pixel array in which a signal is to be read out is turned on, and the read signal is transferred to the floating diffusion. Subsequent operations of the reset transistor **1103**, the amplifier transistor **1104** ~~and the select transistor **1102**~~ are the same as in the description of the upper pixel.

Please amend paragraph [0042] as follows:

[0042] As shown in FIG. **2**, the solid-state imaging apparatus of this embodiment includes photodiodes **1-1-1** through **1-m-n**, transfer transistors **2-1-1** through **2-m-n**, reset transistors **3-1-1** through **3-m-n**, amplifier transistors **4-1-1** through **4-m-n**, [[row]] column signal lines **6-1** through **6-m**, a [[row]] column signal accumulating unit **7**, a column-select unit **8**, a row-select unit **9**, transfer-transistor control lines **10-1** through **10-n**, reset-transistor control lines **11-1** through **11-n**, a load transistor group **13**, and a pixel-section power sources **14**. Herein, m and n are both integers of 2 or more.

Please amend paragraph [0044] as follows:

[0044] The reset-transistor control lines **11-1** through **11-n** are connected to the gates of the reset transistors **3-1-1** through **3-m-n**. The sources of the amplifier transistors **4-1-1** through **4-m-n** are hardwired with [[row]] column signal lines **6-1** through **6-m**, and a load transistor group **13** is formed at respective one ends of the [[row]] column signal lines **6-1** through **6-m**. The [[row]] column signal lines **6-1** through **6-m** are connected at their respective other ends to the [[row]] column signal accumulating unit **7** including a switch transistor for capturing signals from pixels in one row. The [[row]] column signal accumulating unit **7** successively produces final outputs in accordance with ~~row-select~~ column-select pulses supplied from the ~~row-select~~ column-select unit **8**.